LAST MOMENT TUITIONS

Digital Logic Design and Analysis

December 17

Computer Engineering (Semester 3)

Total marks: 80
Total time: 3 Hours

INSTRUCTIONS
(1) Question 1 is compulsory.
*(2) Attempt any **three** from the remaining questions.*
(3) Draw neat diagrams wherever necessary.

1.a. Convert $(1762.46)_{10}$(1762.46)10 into octal, binary and hexadecimal. (3)
b. Prove OR-AND configuration is equivalent to NOR-NOR configuration. (3)
c. perform subtraction using 16's complement. (4)
1. $(CB1)_{16}$(CB1)16 - $(971)_{16}$(971)16
2. $(426)_{16}$(426)16 - $(DBA)_{16}$(DBA)16

d. Find 8's complement of following numbers. (2)
1. $(27)_8$
2. $(321)_8$

e. Perform the following subtraction $(52)_{10}$(52)10 - $(65)_{10}$(65)10 using 2's complement method. (2)
f. Write the hamming code for 1010. (2)
g. Implement the following Boolean equation using NAND gates only.
Y = AB +CDE + F

h. Explain the term prime implicant. (2)

2.a. Design a 4-bit ripple adder. (10)

3.a. Implement a full adder using 8:1 multiplexer. (10)
b. Implement the following functions using demultiplexer. (5)
$F1(A, B, C,) = \Sigma m(0,3,7,)$ $F2(A,B,C) = \Sigma m(1,2,5)$
c. Simplify $F(A,B,C,D) = \Pi M(3,4,5,6,7,10,11,15)$F(A,B,C,D)=ΠM(3,4,5,6,7,10,11,15) (5)
and implement using minimum number of gates.

4.a. Compare TTL and CMOS logic with respect to fan in, fan out, propagation delay, power consumption, noise margin, current and voltage parameters. (5)

b. Draw the circuit for SR flip-flop using two NOR gates and write the architecture body for the same using structural modelling. (5)

c. Explain 1-digit BCD adder. (5)

5.a. Convert JK flip-flop to SR flip-flop and D flip-flop. (10)

b. Design 3-bit synchronous counter using T flip-flop.

6.Write short note on (Any FOUR)

a. State table (5)

b. ALU IC 74181 (5)

c. Sequence Generator (5)

d. Data flow modelling (5)

e. 4-bit ring counter (5)