LAST MOMENT TUITIONS

Digital Logic Design and Analysis

May 18

Computer Engineering (Semester 3)

Total marks: 80
Total time: 3 Hours

INSTRUCTIONS
(1) Question 1 is compulsory.
*(2) Attempt any **three** from the remaining questions.*
(3) Draw neat diagrams wherever necessary.

1.a. Write the entity declaration in VHDL for NOR gate.	(2 marks)
1.b. Add (22)10(22)10 to (56)10(56)10 in BCD.	(2 marks)
1.c. Convert decimal 57 into binary, base 7 and Hexadecimal.	(2 marks)
1.d. Construct Hamming code for 1010.	(2 marks)
1.e. Perform subtraction using 2's complement for (10)10−(7)10(10)10−(7)10 .	(2 marks)
1.f. State and prove De Morgan's law.	(2 marks)
1.g. Convert (77)10(77)10 into Excess-3 code.	(2 marks)
1.h. Perform addition of (34)8(34)8 and (62)8(62)8	(2 marks)
1.i. Find 8's complement of the numbers (37)8(37)8 and (301)8(301)8	(2 marks)
1.j. Explain ASCII code in brief.	(2 marks)

2.a. Simplify the following equation using K map to obtain SOP equation and realize the minimum equation using only NAND gates.
F(A,B,C,D)=Σm(1,2,4,6,9,10,12,14)+d(3,7,13) (10 marks)
2.b. Implement full adder using 8:1 mux. (10 marks)

3.a. Obtain the minimal expression using Quine Mc-Cluskey method
F (A,B,C,D)=Σm(1,2,3,5,6,10,11,13,14)+d(4,7) (10 marks)
3.b. what is race around condition? How to overcome it? (10 marks)

4.a. Design 3 bit asynchronous counter and draw the timing diagram. (10 marks)
4.b. Convert JK flip-flop to SR flip-flop and D flip-flop? (10marks)

5.a. Compare TTL and CMOS with respect to different parameters. (10 marks)
5.b. Explain the features of VHDL and its modelling styles. (10 marks)

Write short notes on (any four)

6.a. Moore and Mealy machine (5 marks)
6.b. Sequence generator (5 marks)
6.c. Universal shift register (5 marks)
6.d. Priority encoder (5 marks)
6.e. Carry look ahead adder (5 marks)