LAST MOMENT TUITIONS

Digital Logic Design and Analysis

Dec 18

Computer Engineering (Semester 3)

Total marks: 80
Total time: 3 Hours

INSTRUCTIONS
(1) Question 1 is compulsory.
*(2) Attempt any **three** from the remaining questions.*
(3) Draw neat diagrams wherever necessary.

1.a. Convert decimal number 576.24 into binary, base-9,Octal, hexadecimal system. (4 marks)
1.b. Construct hamming code for 1010 using odd parity. (4 marks)
1.c. Convert (−89)10(−89)10 to its equivalent Sign Magnitude, 1's complement and 2's Complement Form. (4 marks)
1.d. Perform(BC5)H(BC5)H - (A2B)H(A2B)H without converting to any other base (4 marks)
1.e. Prove De Morgans theorem (4 marks)

2.a. Given the logic expression : $A+B\bar{C}\bar{}+AB\bar{D}\bar{}+ABCDA+B\bar{C}\bar{}+AB\bar{D}\bar{}+ABCD$

1. Express it in standard SOP form.
2. Draw K-map and simplify.
3. Draw logic diagram using NOR gates only. (10 marks)

2.b. Reduce using Quine McClusky method and realise the operations using only NAND gates. F(A,B,C,D)=⊔M(0,2,3,6,7,8,9,12,13)F(A,B,C,D)=⊔M(0,2,3,6,7,8,9,12,13 (10 marks)

3.a. Design a 4-bit binary to gray code converter. (10 marks)
3.b. Design a 4-bit BCD adder using IC 7483 and necessary gates. (10 marks)

4.a. Implement the following logic function using all 4:1 multiplexers with the select inputs as 'B','C','D','E' only.
F(A,B,C,D,E)=Σm(0,1,2,3,6,8,9,10,13,15,17,20,24,30 (10 marks)
4.b. Convert a SR flip-flop to JK flip-flop. (10 marks)

5.a. Design a mod-6 synchronous counter using T FF. (10 marks)
5.b. Explain the operation of 4-bit universal shift register. (10 marks)

Write short notes on any two

6.a. VHDL (10 marks)
6.b. TTL and CMOS logic families (10 marks)
6.c. 4-bit Magnitude compartor. (10 marks)
6.d. 3 to 8 line decoder. (10 marks)